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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,288	06/10/2005	Joachim Christian Reiner	CH02 0037 US	9407

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EXAMINER	
TRAN, MICHAEL THANH	
ART UNIT	**PAPER NUMBER**
2827	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/18/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/538,288	REINER, JOACHIM CHRISTIAN	
	Examiner	Art Unit	
	Michael t. Tran	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,9 and 10* is/are rejected.

7)☒ Claim(s) *2 and 4-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MICHAEL TRAN
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *061005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Communications dated June 10, 2005, claims 1-10 are active in this application.

Foreign Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a) (d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statement filed June 10, 2005 has been considered.

Claim Objections

4. Claims are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections – 35 U.S.C. § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject

matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3 and 9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Fournel et al. [U.S. Patent # 5,943,264] in view of Tsukamoto [U.S. Patent # 6,298,459].

Fournel et al. disclose, in figure 3, a one-time programmable memory device comprising an MOS (metal-oxide semiconductor) selection transistor [M1] and PN diode functioning as memory connected in series between a voltage supply line [V] and ground [Vdd], and further comprising programming means [means coupling to WL] for applying voltages to a gate of said selection transistor, to a gate of said memory transistor and to said voltage supply line, which applied voltages force said memory transistor into a snap-back mode resulting in a current thermally damaging a drain junction of said memory transistor. See Abstract and the "Summary of the Invention" sections.

Fournel et al. disclose all of the above mentioned but is silent about the fact that the memory is a MOS transistor. However, this is not new. Tsukamoto shows that it is well known that a MOS transistor connected diode is functionally equivalent to a pn diode [column 29, lines 1-6]. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Fournel et al. memory element to replace the pn diode for a MOS transistor connected diode as taught by Tsukamoto, since Tsukamoto shows that it is well known in the art that such a substitution is functionally equivalent and that it would enhance the manufacturing process of the memory device.

With respect to claim 3, both Fournel et al. and Tsukamoto disclose that the transistors are NMOS.

With respect to claim 9, Fournel et al. indicated that the memory is applicable to a CMOS technology. See Abstract and the "Background of the Invention" section.

7. Claim 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Fournel et al. [U.S. Patent # 5,943,264] in view of Tsukamoto [U.S. Patent # 6,298,459].

Fournel et al. disclose, in figure 3, a method for programming a one-time programmable memory device comprising an MOS (metal-oxide semiconductor) selection transistor [M1] and PN diode functioning as memory connected in series between a voltage supply line [V] and ground [Vdd], and further comprising programming means [means coupling to WL] for applying voltages to a gate of said selection transistor, to a gate of said memory transistor and to said voltage supply line, which applied voltages force said memory transistor into a snap-back mode resulting in a current thermally damaging a drain junction of said memory transistor. See Abstract and the "Summary of the Invention" sections.

Fournel et al. disclose all of the above mentioned but is silent about the fact that the memory is a MOS transistor. However, this is not new. Tsukamoto shows that it is well known that a MOS transistor connected diode is functionally equivalent to a pn diode [column 29, lines 1-6]. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Fournel et al.

memory element to replace the pn diode for a MOS transistor connected diode as taught by Tsukamoto, since Tsukamoto shows that it is well known in the art that such a substitution is functionally equivalent and that it would enhance the manufacturing process of the memory device.

Allowable Subject Matter

8. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- Programming means comprise means for first applying a predetermined voltage to said gate of said memory transistor and for then ramping down said predetermined voltage applied to said gate of said memory transistor until said memory transistor enters said snap-back mode.
- At least one resistor-capacitor unit arranged between a voltage supply and said gate of said selection transistor and between a voltage and said gate of said memory transistor, said resistor-capacitor unit ensuring that a predetermined voltage is applied to said gate of said selection transistor and said gate of said memory transistor at the earliest a predetermined time after powering up said one-time programmable memory device.
- Programming means require a setup procedure for initiating their operation, which setup procedure comprises more steps than applying one predetermined voltage level to said programming means.

- Programming means apply a programming voltage to said voltage supply line which is higher than a voltage applied to said voltage line for other operations than thermally damaging a drain junction of said memory transistor.
- readout means for applying a high voltage to said gate of said selection transistor, for applying a low voltage to said gate of said memory transistor, for applying a readout voltage to said voltage supply line, for detecting a current through said transistors resulting with said applied voltages, for comparing said detected current with a predetermined current value, and for providing an indication that said memory transistor is programmed in case it is determined that said detected current exceeds said predetermined current value.
- a plurality of memory cells, each of said memory cells including a respective selection transistor and a respective memory transistor connected in series between said voltage supply line and ground, wherein said programming means are suited to apply voltages to said memory cells forcing any selected one of said memory transistors into a snap-back mode resulting in a current thermally damaging a drain junction of the respective memory transistor.

Conclusion

9. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

10. Any inquiry concerning this communication or earlier communications from

the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

11. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit 2827
December 8, 2006

MICHAEL TRAN
PRIMARY EXAMINER